IN THE CLAIMS:

The following listing of claims will replace all prior listings of claims in the application:

1. (Currently Amended): A system, comprising:

a Central Processing Unit (CPU) operatively connected to an external memory and one or more peripherals; and

a Physics Processing Unit (PPU) configured to provide force and collision computations on real-time physics simulation data, wherein the PPU includes:

a PPU Control Engine (PCE) configured to control a physics simulation and to communicate with a PPU software driver executing on the CPU,

a Physics Processing Memory (PPM) coupled to the PPU,

a Data Movement Engine (DME) configured to transfer physics simulation data between the PPM and at least one PPU internal memory in response to commands received from the PCE and to initiate context switches relative to one or more other system elements.

2. (Original): The system of claim 1, wherein the CPU comprises a processing unit resident in a personal computer.

3. (Original): The system of claim 1, wherein the CPU comprises a processing unit resident in a game console.

4. (Original): The system of claim 1, further comprising:

a Graphics Processing Unit (GPU) operatively connected to the CPU.

5. (Currently Amended): The system of claim 1, wherein the CPU and PPU communicate via at least one selected from a group of physical interfaces consisting of: ~~USB~~ Universal Serial Bus (USB), USB2, Firewire, ~~PCI~~ Peripheral Component Interconnect (PCI), ~~PCI-X~~ Peripheral Component Interconnect Extended (PCI-X), PCI-Express, and Ethernet.

6. (Cancelled).

7. (Currently Amended): The system of claim ~~6~~ 1, wherein the PCE comprises programming code stored in a memory resident within the PPU.

8. (Cancelled).

9. (Currently Amended): The system of claim ~~8~~ 1, further comprising:

a Floating Point Engine (FPE) configured to respond ~~responsive~~ to commands from at least one of the PCE and the DME, and to execute ~~executing~~ floating point computations.

10. (Original): The system of claim 9, wherein the PPM comprises high-speed memory and the PPU further comprises a high-speed data bus connecting the high-speed memory to at least one of the DME and the FPE.

11. (Original): The system of claim 10, further comprising:

a memory interface unit managing data communication between the high-speed data bus and the high-speed memory.

12. (Original): The system of claim 10, further comprising:

a processor bus connecting the PCE with at least one physical interface to the CPU.

13. (Original): The system of claim 12, wherein the processor bus is separate from the high-speed bus and connected to the high-speed bus via a bridge.

14. (Currently Amended): The system of claim 9, further comprising:

an Inter-Engine Memory (IEM) coupled to the DME and the FPE and configured to ~~receiving~~ receive physics simulation data from the PPM and to initiate a context switch in response to commands received from the DME.

15. (Currently Amended): The system of claim 14, further comprising:

an Inter-Engine Register (IER) coupled to the DME and the FPE and adapted to initiate DME operation in ~~responsive~~ response to a PCE command.

16. (Currently Amended): The system of claim 14, wherein the IEM comprises ~~is a~~ multiple banks of memory adapted to support parallel threads of execution.

17. (Currently Amended): The system of claim ~~14~~ 15, wherein the IER comprises multiple banks of registers ~~further comprising:~~

~~a multiple register Inter-Engine Register (IER) adapted to initiate DME operation in responsive to a PCE command~~; and,

wherein the IEM comprises ~~is a~~ multiple banks of memory adapted to support two parallel threads of execution.

18. (Original): The system of claim 14, further comprising:

a Scratch Pad Memory (SPM) receiving data from the PPM in response to commands from the DME.

19. (Original): The system of claim 9, further comprising:

a DME control interface comprising:

a first packet queue receiving command packets from the PCE and communicating command packets to the DME; and,

a second packet queue receiving response packets from the DME and communicating the response packets to the PCE.

20. (Currently Amended): The system of claim 16, further comprising:

a Scratch Pad Memory (SPM) configured to receive data from the PPM in response to commands from the DME;

wherein the IEM further comprises a first bank accessible to the DME and a second bank accessible to the FPE; and,

wherein the DME further comprises:

a first unidirectional crossbar connected to the first bank;

a second unidirectional crossbar connected to the second bank; and,

a bi-directional crossbar connecting the first and second crossbars to at least one of the PPM or SPM.

21. (Currently Amended): The system of claim 20, wherein the DME further comprises:

a first Address Generation Unit providing Read address data to the first unidirectional crossbar; and,

a second Address Generation Unit providing Write address data to the second unidirectional crossbar.

22. (Original): The system of claim 10, wherein the FPE further comprises:

a plurality of floating point operation execution units.

23. (Original): The system of claim 22, wherein the plurality of floating point execution units are selectively grouped together to form a vector floating point unit.

24. (Currently Amended): The system of claim 23, wherein the FPE performs floating point operations in ~~responsive~~ response to a Very Long Instruction Word (VLIW).

25. (Currently Amended): A game system, comprising:

a host, wherein the host comprises an external memory and a peripheral operatively connected to a Central Processing Unit (CPU); and,

a Physics Processing Unit (PPU) operatively connected to the CPU and configured to provide force and collision computations on real-time physics simulation data, wherein the PPU includes:

a PPU Control Engine (PCE) configured to control a physics simulation and to communicate with a PPU software driver executing on the CPU,

a Physics Processing Memory (PPM) coupled to the PPU,

a Data Movement Engine (DME) configured to transfer physics simulation data between the PPM and at least one PPU internal memory in response to commands received from the PCE and to initiate context switches relative to one or more other system elements;

wherein the host stores a main game program and a PPU driver; and,

wherein the PPU driver manages all communication between the PPU and the CPU.

26. (Currently Amended): The game system of claim 25, wherein the host further stores:

a first Application Programming Interface (API) associated with the main game program; and

a second API associated with the PPU driver.

27. (Original): The game system of claim 26, wherein the second API is callable by the first API.

28. (Original): The game system of claim 27, wherein the host further comprises a Graphics Processor Unit (GPU), wherein the host further stores:

a GPU driver and a third API associated with the GPU driver;

wherein the second API is callable by the first and third APIs.

29. (Currently Amended): The game system of claim 25, wherein the PPU further comprises a dedicated vector processor adapted to perform parallel floating point operations.

30. (Original): The game system of claim 29, wherein the PPU further comprises a high-speed memory.

31. (Currently Amended): A personal computer system (PC) executing a game program on hardware comprising a memory, a peripheral, and a general purpose microprocessor, the PC further comprising:

a dedicated Physics Processing Unit (PPU) adapted to compute physics simulation data for incorporation within execution of the game program, wherein the PPU includes:

a PPU Control Engine (PCE) configured to control a physics simulation and to communicate with a PPU software driver executing on the general purpose microprocessor,

a Physics Processing Memory (PPM) coupled to the PPU,

a Data Movement Engine (DME) configured to transfer physics simulation data between the PPM and at least one PPU internal memory in response to commands received from the PCE and to initiate context switches relative to one or more other system elements.

32. (Currently Amended): The PC of claim 31, wherein the PPU is operatively connected within the PC by means of ~~a~~ an expansion board.

33. (Original): The PC of claim 32, further comprising a Graphics Processing Unit (GPU) adapted to compute graphics data for incorporation within execution of the game program.

34. (Original): The PC of claim 31, wherein the general purpose microprocessor generates a command in response to execution of the game program and communicates the command to the PPU.

35. (Currently Amended): The PC of claim 34, wherein the PPU and general purpose microprocessor communicate via at least one selected from a group of physical interfaces consisting of ~~USB~~ Universal Serial Bus (USB), USB2, Firewire, ~~PCI~~ Peripheral Component Interconnect (PCI), ~~PCI-X~~ Peripheral Component Interconnect Extended (PCI-X), PCI-Express, and Ethernet.

36. (Original): The PC of claim 35, wherein the PPU comprises a vector processor adapted to run parallel floating point operations.

37. (Currently Amended): The PC of claim 34, wherein the command is a Very Long Instruction Word (VLIW).